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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/762,445
Filing Date: January 22, 2004
Appellant(s): FANG ET AL.

Michael Farjami, Esq.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 3, 2006 appealing from the Office action mailed January 3, 2006

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,147,379	**HORI**	**11-2000**
6,721,205	**KOBAYASHI**	**4-2004**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 6 and 8 – 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori, US 6,147,379 in view of Kobayashi, US 6,721,205.

Regarding claims 1 and 8, Hori teaches a floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

- a stacked gate structure 4 and 6 situated on said substrate 1, said stacked gate structure being situated over a channel region 9 in said substrate (see Fig. 1A);
- a recess 14 formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth (see Fig. 1A);
- a source of said floating gate memory cell 7b situated adjacent to said sidewall of said recess and under said stacked gate structure (see Fig. 1A);
- a Vss connection region 7a situated under said bottom of said recess and under said source (see Fig. 1A), said Vss connection region being connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance (in column 9, lines 64 – 67) wherein said Vss connection region being

situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region thereby preventing an increase in a drain induced barrier lowering (this feature is inherent in Hori since the Vss connection is the bit line connection of the source through which is reference voltage Vs is applied during the operation of the memory cell. Similarly, it will inherently prevent an increase in the drain induced barrier lowering) in between column 8, line 29 and column 9, line 23.

Hori shows the bit line connection in region 7a with reference to Fig. 1A. Hori does not expressly state that the bit line connection is the Vss connection region. Kobayashi clarifies that Vss connection is, in fact, the Vss connection region (column 19, lines 49 – 63). As such, Kobayashi provides the evidence that Hori alone without any structural modification discloses every element claimed.

Regarding claims 2 and 9, Hori teaches reduced lateral diffusion of source causing a reduction in drain induced barrier lowering in said floating gate memory cell since this feature will be inherent due to the structure of the memory cell as shown in Fig. 1A.

Regarding claims 4 and 11, Hori teaches the sidewall of the recess is substantially perpendicular to a top surface of said substrate with reference to Fig. 1A.

Regarding claims 5 and 12, Hori teaches the depth of the recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms in column 8, lines 52 – 56.

Regarding claims 6 and 13, Hori teaches ONO stack situated on the floating gate in column 14, line 14.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Hori, US 6,147,379 in view of Kobayashi, US 6,721,205.

Hori fails to teach the floating gate memory cell is a NOR-type floating gate flash memory cell.

Kobayashi teaches that a memory cell comprising two impurity regions isolated from each other can be adopted for NOR type memory cell array in column 4, lines 17 – 25 for the benefit of reducing the DIBL effect in column 9, lines 7 – 11.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to use Hori's device in NOR type memory cell array for the benefit of reducing the DIBL effect as taught by Kobayashi in column 9, lines 7 – 11.

(10) Response to Argument

The first part of Appellant's arguments (paragraph 3, page 5 through paragraph 1, page 7) can be summarized as follows:

- Hori does not mention a word about lowering ground resistance (or Vss resistance) in the memory array and about the harmful DIBL effects, to which the present invention is directed. Thus, Hori does not teach, disclose, or even suggest the advantageous structure disclosed and claimed by the present invention embodied in independent claims 1 and 8.
- The Examiner has acknowledged that Hori does not address lowering ground resistance (i.e. lowering Vss resistance) in the source region, since and relied on Kobayashi as teaching that Vss connection region is the

source of the memory cell through which the reference voltage is applied during the operation of the memory cell.

- 35 USC 102(b) cannot be used to reject a claim when a combination of two references, instead of a single reference, is relied upon.
- Assuming the Examiner intended to use 35 USC 103(a), Kobayashi is directed to the operation of a memory device without any reference as to a need to reduce DIBL, or the need to reduce the ground resistance, or the need to reduce DIBL while also achieving a reduced ground resistance. Therefore, Kobayashi cannot be combined with Hori, since there is no motivation or suggestion in Kobayashi (or in Hori) to combine one with the other to achieve the present invention.

These arguments are not persuasive for the following reasons.

- The reason why the Examiner did not acknowledge Hori not addressing the lowering of ground resistance (i.e. lowering Vss resistance) in the source region is because this is not a limitation of the claim.
- The Examiner relied on Kobayashi as teaching that Vss connection region is same as Hori's bit line connection, thereby using Kobayashi as a teaching reference. The Appellants are reminded that the rejection was a 102 rejection and therefore no motivation to combine is needed. MPEP section 2131.01 teaches about the use of multiple references under the 102 rejection.

The next part of the Appellant's argument (paragraph 2, page 7 through paragraph 2, page 9) deals with the aspects of Hori's invention and how it is different from that of the Appellants' in teaching away from reducing the DIBL (Drain Induced Barrier Lowering) problem.

Technically, DIBL is the effect of the drain voltage on the output conductance and measured threshold voltage. DIBL occurs in devices where only the gate length is reduced without properly scaling the other dimensions. This effect is due to two – dimensional field distribution at the drain and can typically be eliminated by properly scaling the drain and source depths while increasing the substrate doping density.

In the present case, the independent claims 1 and 8 have both structural limitations and functional limitations.

- The structural limitations are for a floating gate memory cell that has a stacked gate structure situated on a substrate, said stacked gate structure being situated over a channel region in said substrate; a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth; a source of said floating gate memory cell situated adjacent to said sidewall of said recess and under said stacked gate structure; a Vss connection region situated under said bottom of said recess and under said source, said Vss connection region being connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance.

- The functional limitations consist of the Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

Hori's floating gate memory cell (see Fig. 1A) has all the structural limitations of the Appellant's claims. Specifically, Hori discloses a Vss connection region, but does not expressly state *ipsissimis verbis* that the bit line connection is in fact the Vss connection region and therefore anticipates the claims. Kobayashi was not combined to structurally modify Hori in any manner. Rather, Kobayash was cited as a dictionary to further clarify the meaning of Hori's disclosure. See MPEP 2131.01.II to explain the meaning of a term used in the primary referenceshow that Vss connection region is identical to the bit line.

Hori is silent regarding the functional limitations. The Appellant agrees by saying that substantial portion of Hori's "Vss connection region" is at the same elevation level as Hori's source 7b." (see paragraph 2, page 8). This simply means a small part of Hori's "Vss connection region" 7a is situated under the bottom of the recess (14) and under the source 7b. Therefore, the Appellant's assertion that Hori's Vss connection region is not under the source region, as required by the present invention, is not persuasive. The position of the bit line connection 11 shown in Hori's Fig. 1a is electrically equivalent to as being connected to region 7a as the resistivities of the regions 7a, 14 and 15 around the bit line are same.

Furthermore, Appellant has mentioned (last paragraph, page 8 through paragraph 2, page 9) the Examiner's response from the Final Office Action: " the Examiner has also stated that: although, it is possible that Hori's device will not completely eliminate drain induced barrier lowering it will certainly lower it from the highest level developed without the presence of the heavily doped Vss region." Page 6, lines 2 – 5 of the Final Office Action of October 25, 2005".

The Appellant continues to argue that, "as discussed in the present application, according to the presently disclosed and claimed invention, it is not merely the presence of the heavily doped Vss connection region, but it is the position of the heavily doped Vss connection regions, i.e. its position as being fully recessed in relation to the source region, that will reduce the DIBL".

This assertion is also not persuasive, since in absence of actual dopant concentration in the Vss connection region, and the dimension of the recess and the source regions Hori's device will reduce the DIBL for the very same reasons as that of the Appellant. Therefore, the Examiner stands by his response in the Final Office Action.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Asok K. sarkar Asok Kumar Sarkar

June 22, 2006

Primary Examiner

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